REMARKS

Claims 1-4, all the claims pending in the application, stand rejected. Claim 2 has been amended in order to clarify the subject matter of the invention. Applicant has added new claims 5-9 in order to provide a more complete scope of protection.

Claim Rejections - 35 U.S.C. § 102

Claims 1-4 are rejected under 35 U.S.C. § 102(e) as being anticipated by Fei et al. This rejection is traversed for at least the following reasons.

With reference to Fig. 1, the invention as recited in claim 1 is a variable-ordered delta sigma modulator having plural integrators (2, 7, 13) whose outputs (Y_1, Y_2, Y_3) and accompanying quantization errors ($-Q_1$, $-Q_2$, $-Q_3$) are selectively combined by the operation of selectors (Sel, Se2) to form a delta sigma modulator output Y. By such selective combination of integrators, the order of the modulator is thereby varied to create an optimum order with regard to a sampling frequency. As explained at page 1 of the present specification, a unique relationship exists between the SN ratio and order of the delta sigma modulator with regard to sampling frequencies, as illustrated in Fig. 9. Further, the order will depend on the number of integrators used. In the cascaded arrangements illustrated in the several embodiments disclosed in the present application, the output of each integrator supplies an output and a quantization error to a next stage integrator. As explained at pages 7 and 8, a third order delta sigma modulator that supplies quantization error to the integrator in a following stage may be configured. A delta sigma modulator of the fourth order or higher can be made variable by providing a selector to disconnect or connect integrators.

Figure 2 illustrates a block diagram of a fifth order delta sigma modulator. As explained at page 10, a mechanism for switching the order of the delta switching modulator by using selectors may be accomplished by varying the state at which the selectors S1-S7 are connected to the F-terminal. The relationship among the operation of the selectors S1-S7 and the order of the delta sigma modulator is reflected in a table illustrated in Fig. 5. As explained at page 12, on the

basis of such table, a variable-order delta sigma modulator may be implemented without increasing circuit scale.

Finally, with regard to Fig. 7, a delta sigma modulator is illustrated which contains a control means for automatically switching the order into an optimum order in conjunction with the switching of sampling frequencies. A sampling frequency detection unit 42 detects a currently used sampling frequency and a storage unit 43 stores a Table M and a Table N for automatic selection. The Table M shows the combinations between the sampling frequencies and the orders that are optimum to the sampling frequencies (based on Figs. 6 and 9). The Table N shows the connection of the integrators (based on Fig. 5). In operation, the detection unit 42 will detect the sampling frequency and the CPU 41 will consult the Table M and determine the order optimum to the sampling frequency. The CPU then activates the selectors on the basis of Table N in order to realize the delta sigma modulator of the desired order.

The stated relationship between sampling frequency and optimum order of a delta sigma modulator as recited in claim 1, and use of the sampling frequency to switch an order of a delta modulator, including the use of a control means and a table that correlates sampling frequency and optimum order as recited in claim 3, provide a unique advantage to the present invention.

Fei et al

The patent to Fei et al discloses a variable order modulator having a delta-sigma modulator 400 that includes a circuit 407 for selectively varying an order of the modulator to vary the modulation index of the delta sigma modulator (see Abstract). The delta sigma modulator is used in audio devices where a stable "pop guard" is desired in connection with volume control, as explained at col. 3, lines 11-54. In short, the modulator order is varied as a function of input voltage level and not sampling frequency.

Figure 4, which is described at col. 4, lines 6-43, illustrates a delta sigma modulator having a variable order based upon a selective implementation of a set of multiplexers 407 that are provided between integrated stages. As explained at col. 4, lines 27-37, increasing and decreasing the order is implemented by removing or adding integrator stages. A digital embodiment of the delta sigma modulator illustrated in Fig. 5. As explained at col. 4, lines 53-

65, a multiplexer 504 allows the order of the modulator to be changed by selecting between a logic 0 and the output of read multiplexer 503. The patent further notes that when operating in the normal mode, the Mi of the modulator may be dynamically changed in a relatively straight-forward manner.

Nothing in Fei et al teaches the variation of an order of the delta sigma modulator into an optimum order in relation to a sampling frequency. The focus clearly is on voltage level. Thus, the subject matter of claim 1 is not found in Fei et al and the claim cannot be anticipated.

With regard to claim 2, the claim has been amended in order to focus on a relation to sampling frequency, as in claim 1.

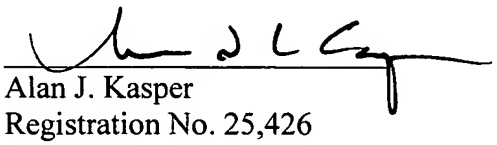
With regard to claims 3 and 4, these claims clearly are distinguishable from the teachings of Fei et al.

Applicant has added new claims 5-9 that state the invention in alternative terminology.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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23373
CUSTOMER NUMBER

Date: June 28, 2004